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# Logic and Computer Design Fundamentals

## Chapter 6 –Selected Design Topics

### Part 2 – Propagation Delay and Timing

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## Overview

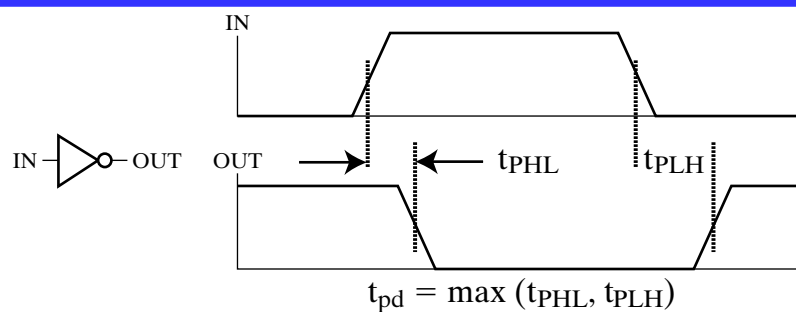
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- **Part 1 – The Design Space**
- **Part 2 – Propagation Delay and Timing**
  - Propagation Delay
  - Delay Models
  - Cost/Performance Tradeoffs
  - Flip-Flop Timing
  - Circuit & System Level Timing
- **Part 3 – Asynchronous Interactions**
- **Part 4 - Programmable Implementation Technologies**

# Propagation Delay

- *Propagation delay* is the time for a change on an input of a gate to propagate to the output.
- Delay is usually measured at the 50% point with respect to the H and L output voltage levels.
- High-to-low ( $t_{PHL}$ ) and low-to-high ( $t_{PLH}$ ) output signal changes may have different propagation delays.
- High-to-low (HL) and low-to-high (LH) transitions are defined with respect to the output, not the input.
- An HL input transition causes:
  - an LH output transition if the gate inverts and
  - an HL output transition if the gate does not invert.

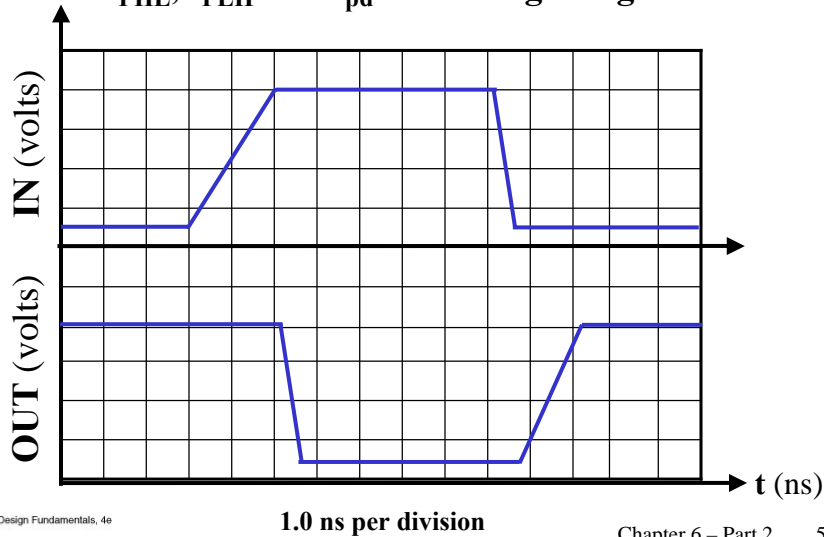
## Propagation Delay (continued)



- Propagation delays measured at the midpoint between the L and H values
- What is the expression for the  $t_{PHL}$  delay for:
  - a string of  $n$  identical buffers?
  - a string of  $n$  identical inverters?

# Propagation Delay Example

- Find  $t_{PHL}$ ,  $t_{PLH}$  and  $t_{pd}$  for the signals given



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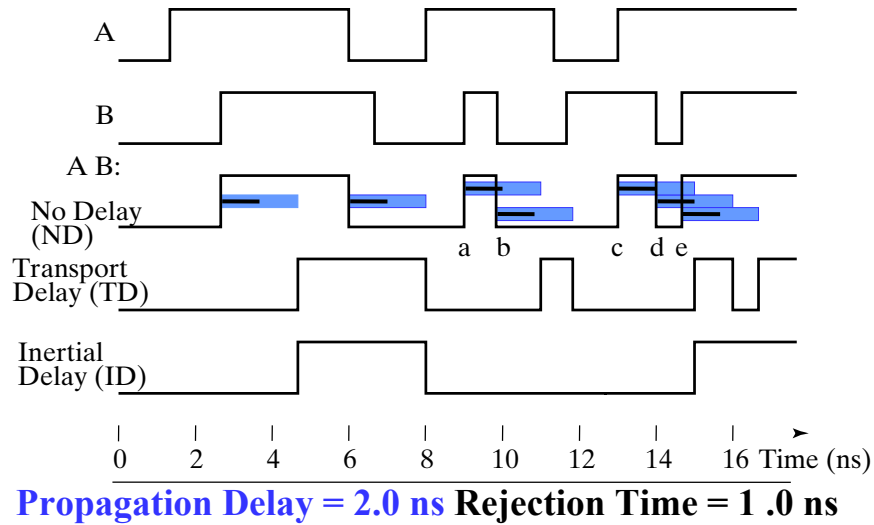
## Delay Models

- Transport delay** - a change in the output in response to a change on the inputs occurs after a fixed specified delay
- Inertial delay** - similar to transport delay, except that if the input changes such that the output is to change twice in a time interval less than the *rejection time*, the output changes do not occur. Models typical electronic circuit behavior, namely, rejects narrow “pulses” on the outputs

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# Delay Model Example

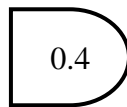


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# Circuit Delay

- Suppose gates with delay  $n$  ns are represented for  $n = 0.2$  ns,  $n = 0.4$  ns,  $n = 0.5$  ns, respectively:



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# Circuit Delay

- Consider a simple 2-input multiplexer:
- With function:
  - $Y = A$  for  $S = 1$
  - $Y = B$  for  $S = 0$

- “Glitch” is due to delay of inverter

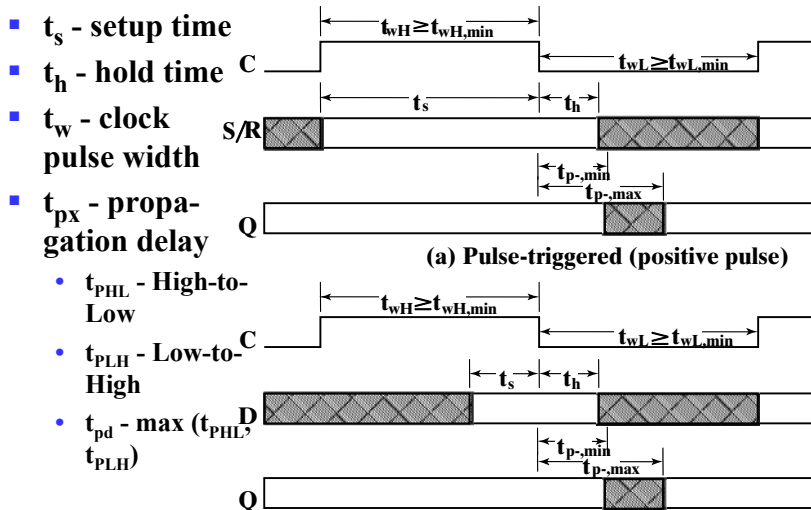
# Fan-out and Delay

- The fan-out loading a gate’s output affects the gate’s propagation delay
- Example:
  - One realistic equation for  $t_{pd}$  for a NAND gate with 4 inputs is:
 
$$t_{pd} = 0.07 + 0.021 SL \text{ ns}$$
  - SL is the number of standard loads the gate is driving, i. e., its fan-out in standard loads
  - For  $SL = 4.5$ ,  $t_{pd} = 0.165 \text{ ns}$
- If this effect is considered, the delay of a gate in a circuit takes on different values depending on the circuit load on its output.

# Cost/Performance Tradeoffs

- **Gate-Level Example:**
  - NAND gate G with 20 standard loads on its output has a delay of 0.45 ns and has a normalized cost of 2.0
  - A buffer H has a normalized cost of 1.5. The NAND gate driving the buffer with 20 standard loads gives a total delay of 0.33 ns
  - In which of the following cases should the buffer be added?
    1. The cost of this portion of the circuit cannot be more than 2.5
    2. The delay of this portion of the circuit cannot be more than 0.40 ns
    3. The delay of this portion of the circuit must be less than 0.30 ns and the cost less than 3.0
- Tradeoffs can also be accomplished much higher in the design hierarchy
- Constraints on cost and performance have a major role in making tradeoffs

# Flip-Flop Timing Parameters

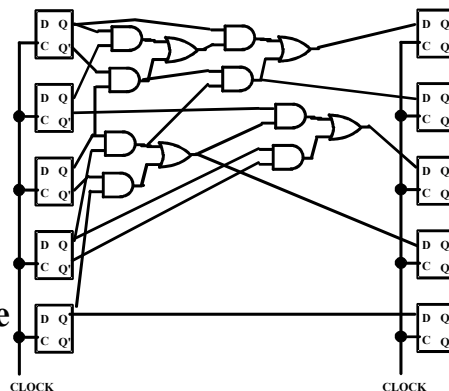


# Flip-Flop Timing Parameters

- $t_s$  - setup time
  - Master-slave - Equal to the width of the triggering pulse
  - Edge-triggered - Equal to a time interval that is generally much less than the width of the triggering pulse
- $t_h$  - hold time - Often equal to zero
- $t_{px}$  - propagation delay
  - Same parameters as for gates except
  - Measured from clock edge that triggers the output change to the output change

## Circuit and System Level Timing

- Consider a system comprised of ranks of flip-flops connected by logic:
- If the clock period is too short, some data changes will not propagate through the circuit to flip-flop inputs before the setup time interval begins

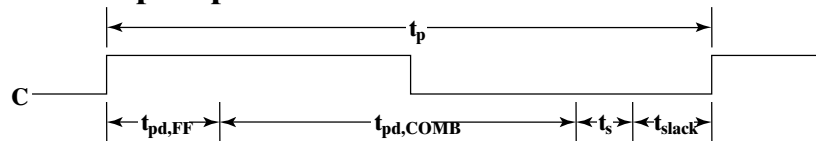


# Circuit and System Level Timing

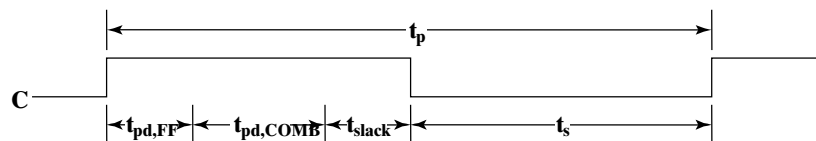
- **New Timing Components**
  - $t_p$  - clock period - The interval between occurrences of a specific clock edge in a periodic clock
  - $t_{pd,COMB}$  - total delay of combinational logic along the path from flip-flop output to flip-flop input
  - $t_{slack}$  - extra time in the clock period in addition to the sum of the delays and setup time on a path
    - Can be either positive or negative
    - Must be greater than or equal to zero on all paths for correct operation

# Circuit and System Level Timing

- **Timing components along a path from flip-flop to flip-flop**



(a) Edge-triggered (positive edge)



(b) Pulse-triggered (negative pulse)

# Circuit and System Level Timing

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- **Timing Equations**

$$t_p = t_{\text{slack}} + (t_{\text{pd,FF}} + t_{\text{pd,COMB}} + t_s)$$

- For  $t_{\text{slack}}$  greater than or equal to zero,

$$t_p \geq \max(t_{\text{pd,FF}} + t_{\text{pd,COMB}} + t_s)$$

for all paths from flip-flop output to flip-flop input

- **Can be calculated more precisely by using  $t_{\text{PHL}}$  and  $t_{\text{PLH}}$  values instead of  $t_{\text{pd}}$  values, but requires consideration of inversions on paths**

## Calculation of Allowable $t_{\text{pd,COMB}}$

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- **Compare the allowable combinational delay for a specific circuit:**
  - a) Using edge-triggered flip-flops
  - b) Using master-slave flip-flops
- **Parameters**
  - $t_{\text{pd,FF}}(\text{max}) = 1.0 \text{ ns}$
  - $t_s(\text{max}) = 0.3 \text{ ns}$  for edge-triggered flip-flops
  - $t_s = t_{\text{wH}} = 1.0 \text{ ns}$  for master-slave flip-flops
  - Clock frequency = 250 MHz

## Calculation of Allowable $t_{pd,COMB}$

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- **Calculations:  $t_p = 1/\text{clock frequency} = 4.0 \text{ ns}$** 
  - **Edge-triggered:  $4.0 \geq 1.0 + t_{pd,COMB} + 0.3$ ,  $t_{pd,COMB} \leq 2.7 \text{ ns}$**
  - **Master-slave:  $4.0 \geq 1.0 + t_{pd,COMB} + 1.0$ ,  $t_{pd,COMB} \leq 2.0 \text{ ns}$**
- **Comparison: Suppose that for a gate, average  $t_{pd} = 0.3 \text{ ns}$** 
  - **Edge-triggered: Approximately 9 gates allowed on a path**
  - **Master-slave: Approximately 6 to 7 gates allowed on a path**

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