
Logic and Computer Design Fundamentals

Chapter 6 – Selected Design Topics

Part 3 – Asynchronous Interactions

Charles Kime & Thomas Kaminski

© 2008 Pearson Education, Inc.
(Hyperlinks are active in View Show mode)

Overview

- **Part 1 – The Design Space**
- **Part 2 – Propagation Delay and Timing**
- **Part 3 – Asynchronous Interactions**
 - **Types of Interactions**
 - **Combinational Hazards**
 - **Synchronization**
 - **Metastability**
 - **Synchronous Circuit Pitfalls**
- **Part 4 - Programmable Implementation Technologies**

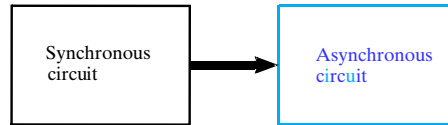
Types of Interactions

- **Differ by**
 - Source circuit type
 - Destination circuit type
- **Sequential circuit types**
 - Synchronous – time of state change determined by a clock
 - Asynchronous – time of state change controlled by time of input changes and combinational circuit delay
- **Four possible pairings**
 - Asynchronous to Asynchronous
 - Synchronous to Asynchronous
 - Asynchronous to Synchronous
 - Synchronous to Synchronous

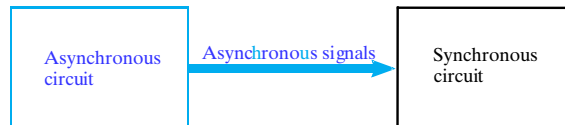
Types of Interactions

- **Asynchronous to Asynchronous – not of concern since we are not covering general asynchronous circuit design**
- **Synchronous to Asynchronous – synchronous circuit outputs must be free of hazards**
- **Asynchronous to Synchronous – inputs must be *synchronized* to synchronous circuit clock**
- **Synchronous to Synchronous**
 - Clocks synchronized with each other (including identical) – normal clock timing constraints must be obeyed.
 - Clocks not synchronized – inputs must be *synchronized* to receiving synchronous circuit's clock

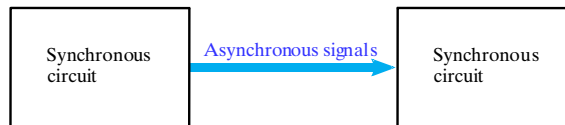
Types of Interactions



(a) Synchronous to asynchronous



(b) Asynchronous to synchronous



(c) Synchronous circuits with unrelated clocks

Logic and Computer Design Fundamentals, 4e
PowerPoint® Slides
© 2008 Pearson Education, Inc.

Chapter 6 – Part 3 5

Synchronous to Asynchronous

- Since the asynchronous circuit state changes in response to input changes, there must be no “glitches” in the outputs of the synchronous circuit.
- Such glitches can arise from:
 - combinational output logic or
 - input signals propagating through the synchronous circuit
- In order to avoid “glitches”
 - the outputs of the synchronous circuit must be Moore outputs, and
 - The output logic driving the asynchronous circuit must be free of combinational logic hazards
- Satisfying these two requirements is too complex for consideration here and is covered in the reading supplement *Combinational Hazards*.

Logic and Computer Design Fundamentals, 4e
PowerPoint® Slides
© 2008 Pearson Education, Inc.

Chapter 6 – Part 3 6

Remaining Interactions

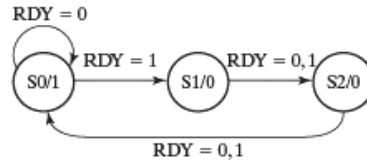
- **Includes asynchronous circuits to synchronous circuits and synchronous circuits to synchronous circuits with unsynchronized clocks**
- **The problem: Input signal changes arrive at flip-flop inputs during the setup time – hold time interval.**
- **The solution:**
 - Synchronize input signals with the receiving circuit clock
 - Otherwise, guarantee that specific input signals will not arrive at flip-flop inputs during the setup time – hold time interval.
 - We will focus on the first approach only.

The Problem

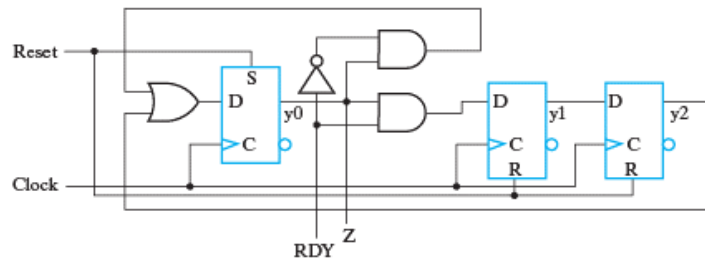
- **Changes in inputs to a synchronous circuit arrive at inputs to two or more circuit flip-flops during the setup-hold time interval. (For simplicity, D flip-flops are assumed.)**
- **When this occurs, the flip-flops may respond differently, e.g., one flip-flop may change its state and another may not change its state, resulting in an incorrect state.**

Problem Example

- Both illustrations use the same circuit



(a) State diagram



(b) Logic diagram

Logic and Computer Design
PowerPoint® Slides
© 2008 Pearson Education, Inc.

Problem Example

- Both illustrations use the same circuit
- The circuit has three states and uses a 1-hot state assignment:
- The circuit interacts with its environment using two signals, Z and RDY. When the circuit enters state S0, it signals to the environment with Z = 1. In response, the environment signals back that it is ready to move to state S1 with asynchronous input RDY = 1.

State	State Variable = 1
S0	y0
S1	y1
S2	y2

Logic and Computer Design Fundamentals, 4e
PowerPoint® Slides
© 2008 Pearson Education, Inc.

Illustration 1 of the Problem

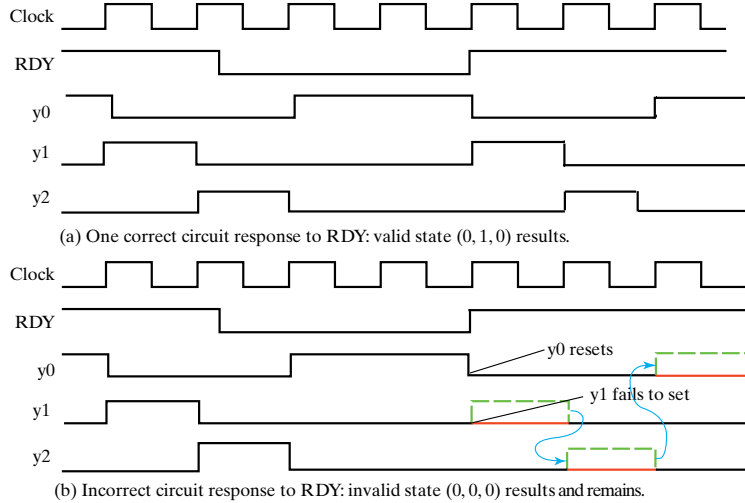
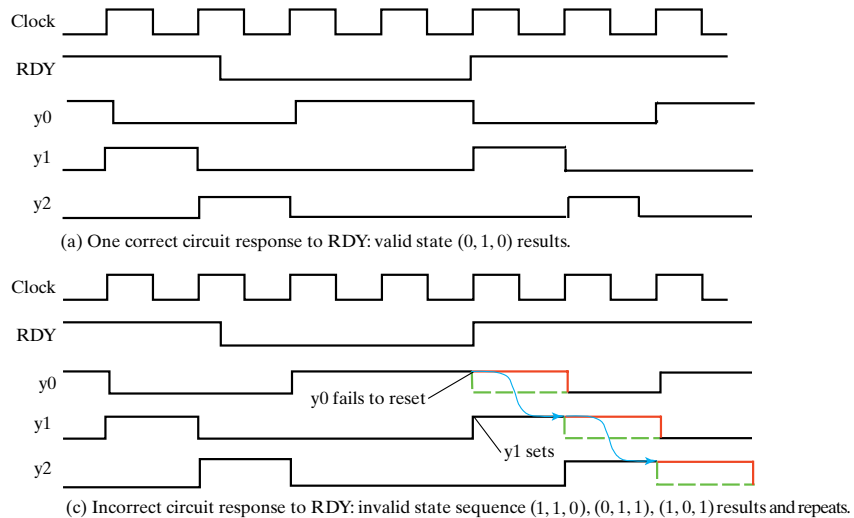


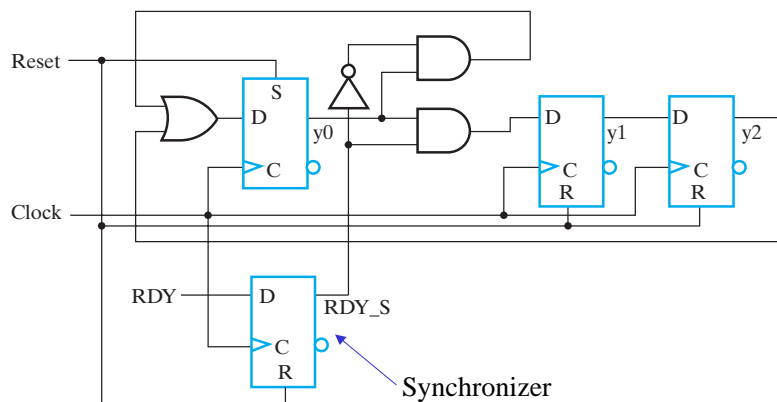
Illustration 2 of the Problem



Solution using Synchronizers

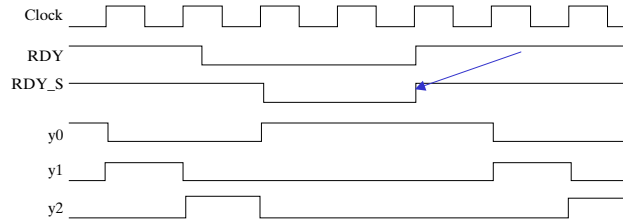
- **Goal of solution: Preventing the inconsistent response of two or more flip-flops to the change in RDY by preventing RDY from reaching the input of more than one circuit flip-flop.**
- **Implementation: Place a D flip-flop in the path from RDY to the circuit.**

Example Circuit with Synchronizer

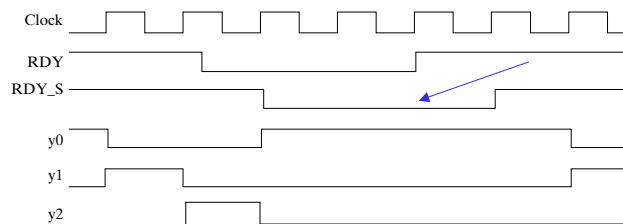


Circuit Behavior with Synchronizer

- Assumption 1: If RDY changes during setup-hold interval, synchronizer either responds with corresponding change or not.



(a) Circuit response to RDY with sensing at the Clock edge where RDY changes

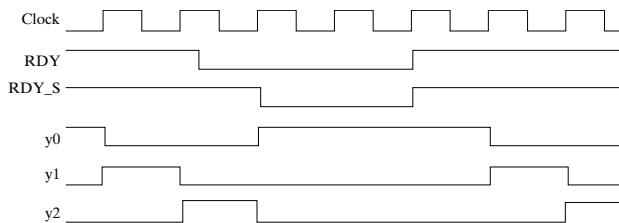


(b) Circuit response to RDY with sensing at the next Clock edge where RDY changes Chapter 6 – Part 3 15

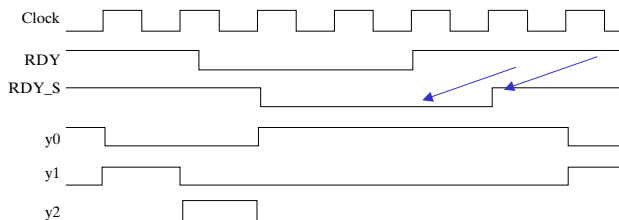
Logic and Computer
PowerPoint® Slides
© 2008 Pearson Education, Inc.

Circuit Behavior with Synchronizer

- Assumption 2: If RDY change missed during setup-hold interval, change will be captured at next clock edge.



(a) Circuit response to RDY with sensing at the Clock edge where RDY changes



(b) Circuit response to RDY with sensing at the next Clock edge where RDY changes Chapter 6 – Part 3 16

Logic and Comput
PowerPoint® Slide
© 2008 Pearson Education, Inc.

Circuit Behavior with Synchronizer

- **Condition 1:** In order to allow the previous pair of situations to capture the changed value of RDY, the time interval at which RDY retains its new value is constrained as follows:

$$t_{RDY} > t_s + t_p + t_h$$

in which t_s is the setup time, t_p is the clock period and t_h is the hold time.

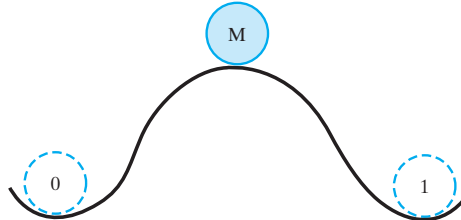
- The time at which RDY is captured may differ by a clock cycle. Since the timing of the asynchronous circuit signal RDY is unknown with respect to the clock, the circuit must be designed to work correctly within this capture variation, including capture variation of multiple asynchronous inputs.

Metastability

- Unfortunately, Assumption 1 given earlier is not correct. The synchronizer does not respond to an input change during the setup-hold interval by either changing or not.
- If the change in RDY at the D input to the synchronizer flip-flop occurs in a very small window within the setup-hold time interval, then *metastable behavior* can occur.
- The window width is of the order of 10 picoseconds (pico = 10^{-12}).

Metastability Concept

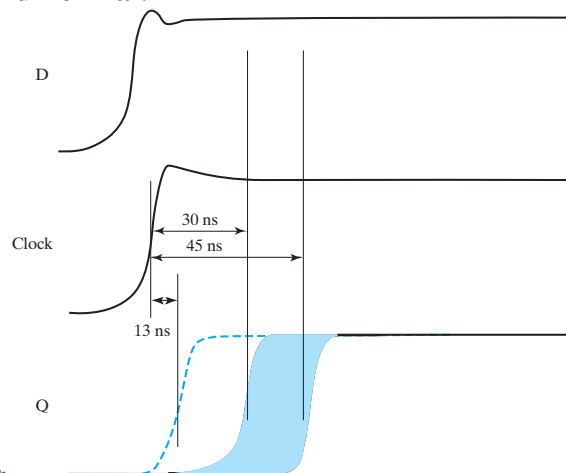
- The concept of metastability can be illustrated by a mechanical analogy



- In positions 0 and 1, the ball is stopped in a stable state. In position M, the ball is stopped in a unstable state between 0 and 1 and remains there until perturbed by, for example, the wind.
- The metastable state in a flip-flop latch can be attained by logical ANDing of the RDY change close to a Clock change that produces a very weak output pulse.
- Departure from the metastable state is produced by electronic “noise” injected into the flip-flop latch

Metastable Behavior

- Metastability lengthens the propagation delay to well beyond normal.



Metastable Behavior Consequences

- **If the clock period is short enough, due to the increase in delay, the change in RDY_S may reach the D inputs to the y0 and y1 flip-flops during the setup-hold interval at the next positive edge and produce inconsistent behavior.**
- **So, metastable behavior can reintroduce a failure in spite of the presence of the synchronizer.**

Solution to Metastable Behavior

- **Simple Solution: A Cascade of Synchronizers**
 - **The metastable behavior delay of the first synchronizer is encountered by the next synchronizer.**
 - **Due to the narrow window, it is unlikely that the next synchronizer also exhibits metastable behavior**
 - **And so forth**
- **Clearly each added synchronizer lowers probability of failure rather than absolutely eliminating failure**
- **Disadvantage: May slow response to asynchronous input due to multiple clock cycles required for production of final RDY_S.**
- **Typically, a cascade of three synchronizers in series lowers probability adequately, but depends on clock period, delays, etc.**

Terms of Use

- **All (or portions) of this material © 2008 by Pearson Education, Inc.**
- **Permission is given to incorporate this material or adaptations thereof into classroom presentations and handouts to instructors in courses adopting the latest edition of Logic and Computer Design Fundamentals as the course textbook.**
- **These materials or adaptations thereof are not to be sold or otherwise offered for consideration.**
- **This Terms of Use slide or page is to be included within the original materials or any adaptations thereof.**