
Logic and Computer Design Fundamentals

Chapter 9 – Computer Design Basics

Part 3 – Multiple-Cycle Hardwired Control

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Overview

- **Part 1 – Datapaths**
- **Part 2 – A Simple Computer**
- **Part 3 – Multiple Cycle Hardwired Control**
 - **Single Cycle Computer Issues**
 - **Modifications to Datapath**
 - **Modifications to Control**
 - **Sequential Control Design**

Single-Cycle Computer Issues

- **Shortcoming of Single Cycle Design**
 - **Complexity of instructions executable in a single cycle is limited**
 - **Accessing both an instruction and data from a simple single memory impossible**
 - **A long worst case delay path limits clock frequency and the rate of performing instructions**
- **Handling of Shortcomings**
 - **The first two shortcomings can be handled by the multiple-cycle computer discussed here**
 - **The third shortcoming is dealt with by using a technique called pipelining described in Chapter 12**

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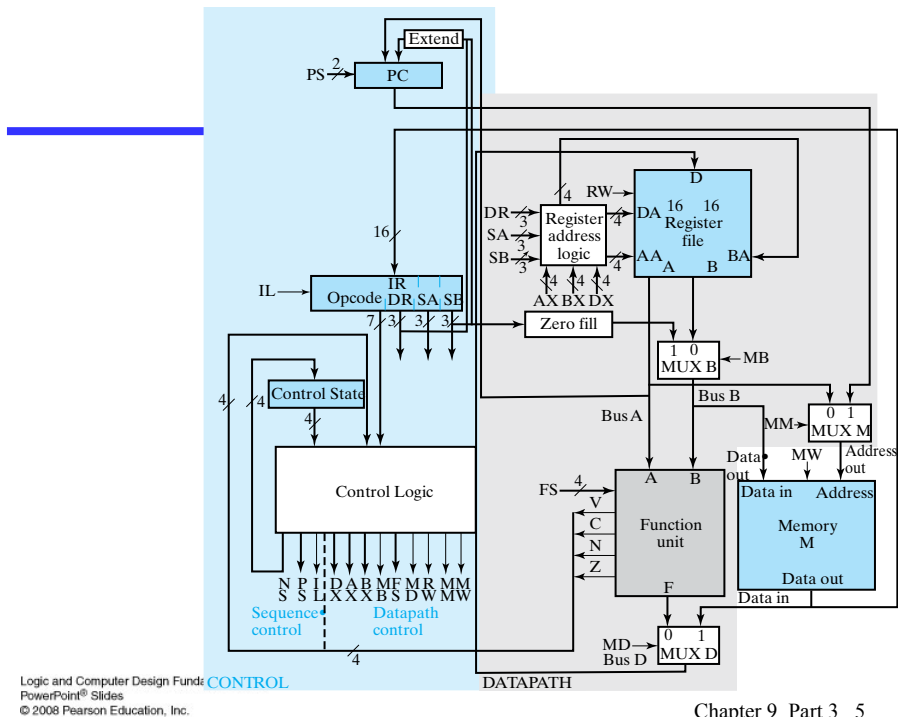
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Multiple-Cycle Computer

- **Converting the single-cycle computer into a multiple-cycle computer involves:**
 - **Modifications to the datapath/memory**
 - **Modification to the control unit**
 - **Design of a multiple-cycle hardwired control**
- **The block diagram of the single-cycle SC architecture is given on the next slide for use in developing the multiple-cycle SC architecture**

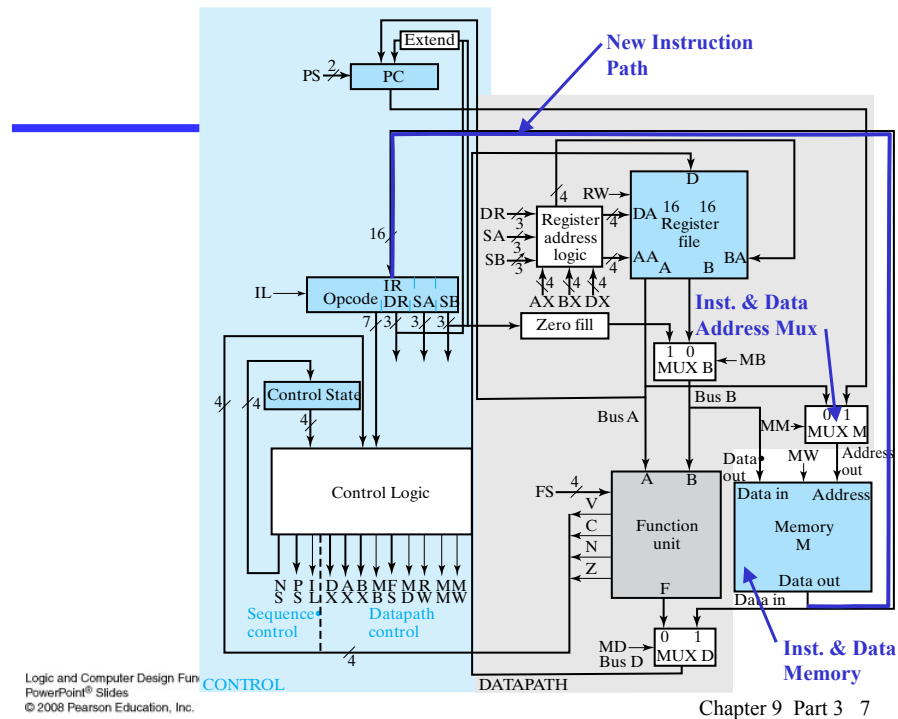
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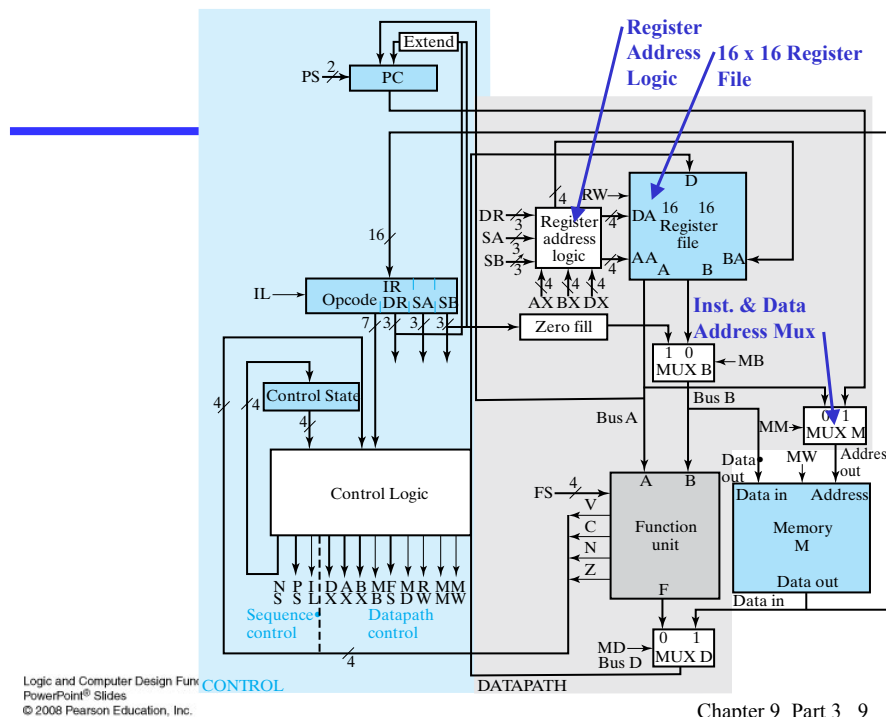
Datapath Modifications

- **Modifications appear on the next slide**
- **Use a single memory for both instructions and data**
 - **Not essential to the multiple-cycle design, but done to illustrate the concept**
 - **Requires new MUX M with control signal MM to select the instruction address from the PC or the data address**
 - **Requires path from Memory Data Out to the instruction path in the control unit**



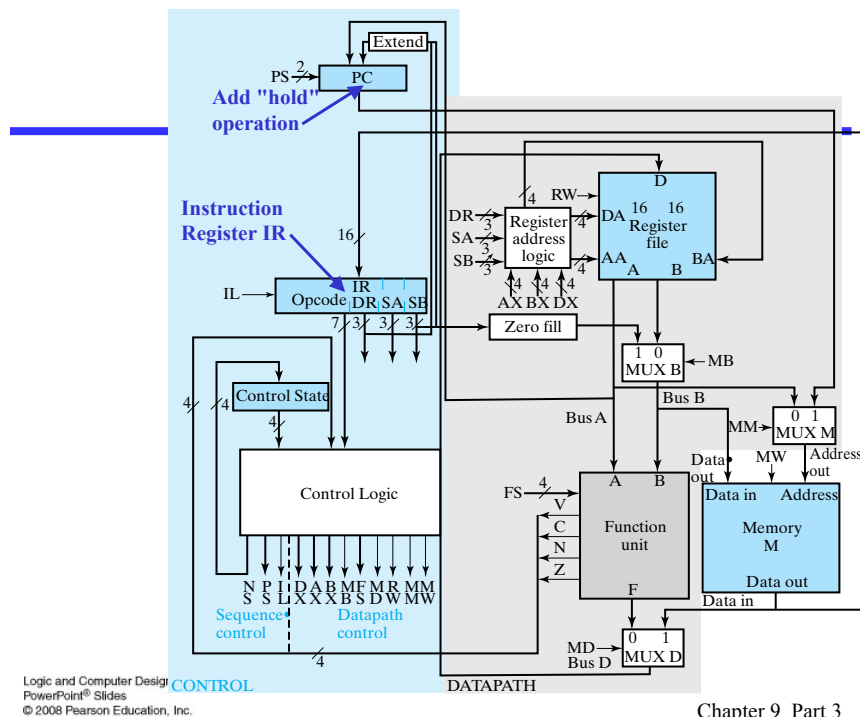
Datapath Modifications (continued)

- To hold operands between cycles, need additional registers
 - Add 8 temporary storage registers to the Register File
 - Register File becomes 16 x 16
 - Addresses to Register File increase from 3 to 4 bits
 - Register File addresses come from:
 - The instruction for the Storage Resource registers (0 to 7)
 - The control word for the Temporary Storage registers (8 to 15)
 - The control word specifies the source for Register File addresses
 - Add Register Address Logic to the Register File to select the register address sources
 - Three new control fields for register address source selection and temporary storage addressing: DX, AX, BX



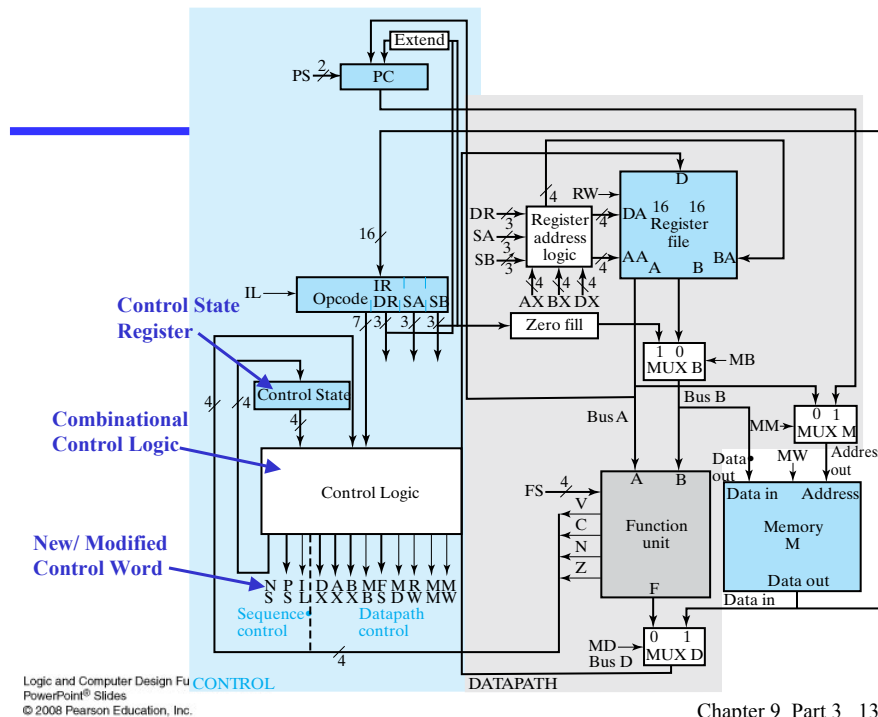
Control Unit Modifications

- **Must hold instruction over the multiple cycles to draw on instruction information throughout instruction execution**
 - **Requires an Instruction Register (IR) to hold the instruction**
 - Load control signal IL
 - **Requires the addition of a "hold" operation to the PC since it only counts up to obtain a new instruction**
 - New encoding for the PC operations uses 2 bits



Sequential Control Design

- **In order to control microoperations over multiple cycles, a Sequential Control replaces the Instruction Decoder**
 - **Input:** Opcode, Status Bits
 - **Output:** Control Word (Modified Datapath Control part)
 - **Control State**
 - **Next State:** Control Word (New Sequencing Control part)
 - **Consists of (see next slide):**
 - **Register to store the Control State**
 - **Combinational Logic to generate the Control Word (both sequencing and datapath control parts)**
 - **The Combinational Logic is quite complex so we assume that it is implemented by using a PLA or synthesized logic and focus on ASM level design**



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Control Word

27	24	23	22	21	20	17	16	13	12	9	8	7	4	3	2	1	0
NS	PS	I	DX	AX	BX	M	B	FS	M	R	M	M	D	W	M	M	W

Sequencing

Datapath

- **Datapath part: fields DA, AA, and BA replaced by DX, AX, and BX, respectively, and field MM added**
 - If the MSB of a field is 0, e.g., AX = 0XXX, then AA is 0 concatenated with 3 bits obtained from the SA field in the IR
 - If the MSB of a field is 1, e.g. AX = 1011, then AA = 1011
- **Sequencing part:**
 - IL controls the loading of the IR
 - PS controls the operations of the PC
 - NS gives the next state of the Control State register
 - NS is 4 bits, the length of the Control State register - 16 states are viewed as adequate for this design

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Encoding for Datapath Control

DX	AX	BX	Code	MB	Code	FS	Code	MD	RW	MM	MW	Code
<i>R</i> [DR]	<i>R</i> [SA]	<i>R</i> [SB]	0XXX	Register	0	$F \leftarrow A$	0000	FnUt	No write	Address Out	No write	0
<i>R8</i>	<i>R8</i>	<i>R8</i>	1000	Constant	1	$F \leftarrow A + 1$	0001	Data In	Write	PC	Write	1
<i>R9</i>	<i>R9</i>	<i>R9</i>	1001			$F \leftarrow A + B$	0010					
<i>R10</i>	<i>R10</i>	<i>R10</i>	1010			Unused	0011					
<i>R11</i>	<i>R11</i>	<i>R11</i>	1011			Unused	0100					
<i>R12</i>	<i>R12</i>	<i>R12</i>	1100			$F \leftarrow A + \overline{B} + 1$	0101					
<i>R13</i>	<i>R13</i>	<i>R13</i>	1101			$F \leftarrow A - 1$	0110					
<i>R14</i>	<i>R14</i>	<i>R14</i>	1110			Unused	0111					
<i>R15</i>	<i>R15</i>	<i>R15</i>	1111			$F \leftarrow A \wedge B$	1000					
						$F \leftarrow A \vee B$	1001					
						$F \leftarrow A \oplus B$	1010					
						$F \leftarrow \overline{A}$	1011					
						$F \leftarrow B$	1100					
						$F \leftarrow sr B$	1101					
						$F \leftarrow sl B$	1110					
						Unused	1111					

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Encoding for Sequencing Control

	NS	PS		IL	
	Next State	Action	Code	Action	Code
Gives next state of Control State Register	Hold PC	00	No load	0	
	Inc PC	01	Load IR	1	
	Branch	10			
	Jump	11			

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SMDs for Sequential Control

- **An instruction requires two steps:**
 - *Instruction fetch* – obtaining an instruction from memory
 - *Instruction execution* – the execution of a sequence of microoperations to perform instruction processing
 - Due to the use of the IR, these two steps require a minimum of two clock cycles
- **ISA: Instruction Specifications and SMD for the instructions (that all require two clock cycles) are given on the next four slides.**

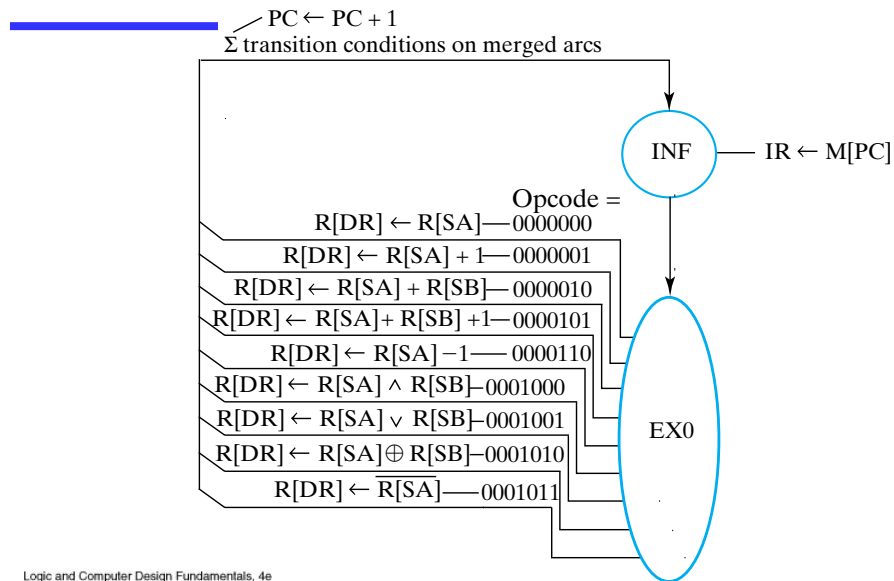
ISA: Instruction Specifications (for reference only)

Instruction Specifications for the SimpleComputer - Part 1

Instruction	Opcode	Mnemonic	Format	Description	Status Bits
Move A	0000000	MOVA	RD,RA	$R[DR] \leftarrow R[SA]$	N, Z
Increment	0000001	INC	R D,RA	$R[DR] \leftarrow R[SA] + 1$	N, Z
Add	0000010	ADD	R D,RA,RB	$R[DR] \leftarrow R[SA] + R[SB]$	N, Z
Subtract	0000101	SUB	R D,RA,RB	$R[DR] \leftarrow R[SA] - R[SB]$	N, Z
Decrement	0000110	DEC	R D,RA	$R[DR] \leftarrow R[SA] - 1$	N, Z
AND	0001000	AND	R D,RA,RB	$R[DR] \leftarrow R[SA] \wedge R[SB]$	N, Z
OR	0001001	OR	R D,RA,RB	$R[DR] \leftarrow R[SA] \vee R[SB]$	N, Z
Exclusive OR	0001010	XOR	R D,RA,RB	$R[DR] \leftarrow R[SA] \oplus R[SB]$	N, Z
NOT	0001011	NOT	R D,RA	$R[DR] \leftarrow \overline{R[SA]}$	N, Z

- **SMD on Next Slide**

SMD for Two-Cycle Instructions - Part 1



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ISA: Instruction Specifications (for reference only)

Instruction Specifications for the Simple Computer - Part 2

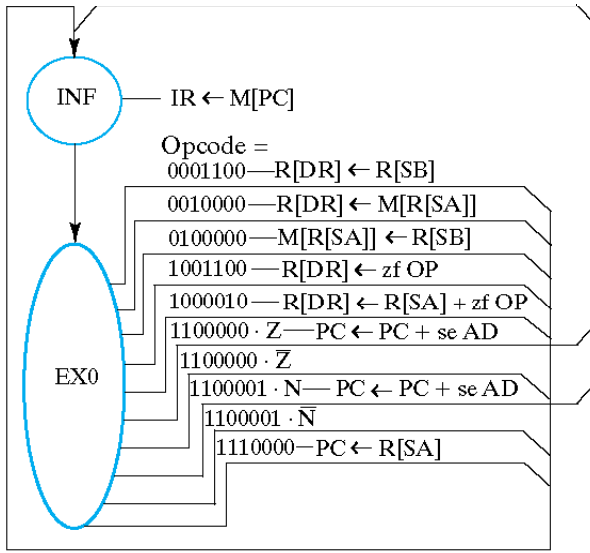
Instruction	Opcode	Mnemonic	Format	Description	Status Bits
Move B	0001100	MOVB	RD,RB	$R[DR] \leftarrow R[SB]$	
Shift Right	0001101	SHR	RD,RB	$R[DR] \leftarrow sr R[SB]$	
Shift Left	0001110	SHL	RD,RB	$R[DR] \leftarrow sl R[SB]$	
Load Immediate	1001100	LDI	RD,OP	$R[DR] \leftarrow zf OP$	
Add Immediate	1000010	ADI	RD,RA,OP	$R[DR] \leftarrow R[SA] + zf OP$	
Load	0010000	LD	RD,RA	$R[DR] \leftarrow M[SA]$	
Store	0100000	ST	RA,RB	$M[SA] \leftarrow R[SB]$	
Branch on Zero	1100000	BRZ	RA,AD	if $(R[SA] = 0)$ $PC \leftarrow PC + se AD$	
Branch on Negative	1100001	BRN	RA,AD	if $(R[SA] < 0)$ $PC \leftarrow PC + se AD$	
Jump	1110000	JMP	RA	$PC \leftarrow R[SA]$	

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SMD for 2-Cycle Instructions – Part 2

- Instruction Fetch Portion Duplicated From Part 1



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PC ← PC + 1
Σ transition conditions on merged arcs

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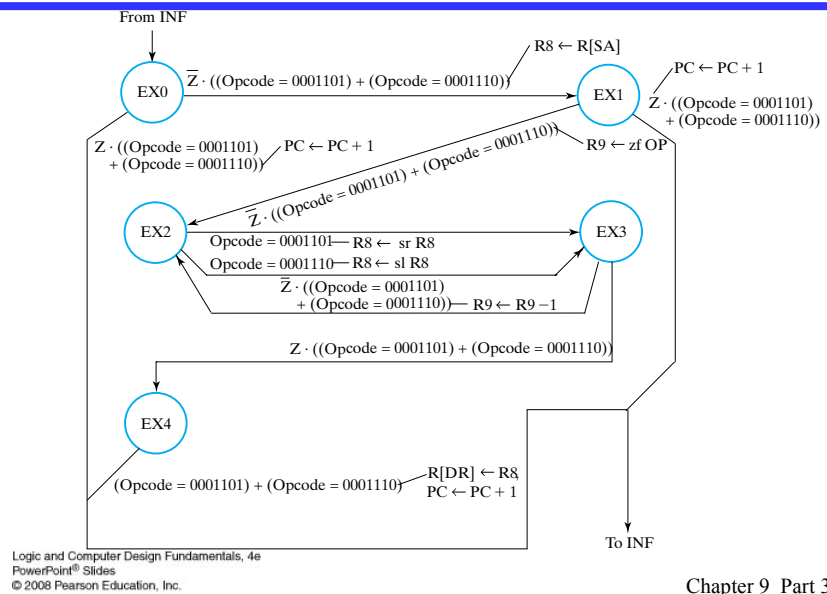
State Table for 2-Cycle Instructions

State	Inputs		Next state	Outputs												Comments
	Opcode	VCNZ		I L	P S	DX	AX	BX	M B	FS	M D	R W	M W	M W		
INF	XXXXXX	XXXX	EX0	1	00	XXX	XXX	XXX	X	XXX	X	0	1	0	IR ← M[PC]	
EX0	0000000	XXXX	INF	0	01	0XXX	0XXX	0XXX	X	0000	0	1	X	0	MOVA R[DR] ← R[SA]*	
EX0	0000001	XXXX	INF	0	01	0XXX	0XXX	0XXX	X	0001	0	1	X	0	INC R[DR] ← R[SA] + 1*	
EX0	0000010	XXXX	INF	0	01	0XXX	0XXX	0XXX	0	0010	0	1	X	0	ADD R[DR] ← R[SA] + R[SB]*	
EX0	0000101	XXXX	INF	0	01	0XXX	0XXX	0XXX	0	0101	0	1	X	0	SUB R[DR] ← R[SA] - R[SB]*	
EX0	0000110	XXXX	INF	0	01	0XXX	0XXX	0XXX	X	0110	0	1	X	0	DEC R[DR] ← R[SA] - 1*	
EX0	0001000	XXXX	INF	0	01	0XXX	0XXX	0XXX	0	1000	0	1	X	0	AND R[DR] ← R[SA] & R[SB]*	
EX0	0001001	XXXX	INF	0	01	0XXX	0XXX	0XXX	0	1001	0	1	X	0	OR R[DR] ← R[SA] R[SB]*	
EX0	0001010	XXXX	INF	0	01	0XXX	0XXX	0XXX	0	1010	0	1	X	0	XOR R[DR] ← R[SA] ⊕ R[SB]*	
EX0	0001011	XXXX	INF	0	01	0XXX	0XXX	0XXX	X	1011	0	1	X	0	NOT R[DR] ← ~R[SA]*	
EX0	0001100	XXXX	INF	0	01	0XXX	0XXX	0XXX	0	1100	0	1	X	0	MOVB R[DR] ← R[SB]*	
EX0	0010000	XXXX	INF	0	01	0XXX	0XXX	0XXX	X	XXXX	1	1	0	0	LD R[DR] ← M[R[SA]]*	
EX0	0100000	XXXX	INF	0	01	0XXX	0XXX	0XXX	0	XXXX	X	0	0	1	ST M[R[SA]] ← R[SB]*	
EX0	1001100	XXXX	INF	0	01	0XXX	0XXX	0XXX	1	1100	0	1	0	0	LDI R[DR] ← zf OP*	
EX0	1000010	XXXX	INF	0	01	0XXX	0XXX	0XXX	1	0010	0	1	0	0	ADI R[DR] ← R[SA] + zf OP*	
EX0	1100000	XXX	INF	0	10	0XXX	0XXX	0XXX	X	0000	X	0	0	0	BRZ PC ← PC + se AD	
EX0	1100000	XXX0	INF	0	01	0XXX	0XXX	0XXX	X	0000	X	0	0	0	BRZ PC ← PC + 1	
EX0	1100001	XX1X	INF	0	10	0XXX	0XXX	0XXX	X	0000	X	0	0	0	BRN PC ← PC + se AD	
EX0	1100001	XX0X	INF	0	01	0XXX	0XXX	0XXX	X	0000	X	0	0	0	BRN PC ← PC + 1	
EX0	1110000	XXXX	INF	0	11	0XXX	0XXX	0XXX	X	0000	X	0	0	0	JMP PC ← R[SA]	

* For this state, a transition to the next state occurs.
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SMD for Right Shift and Left Shift Multiple



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State Table For Right and Left Shift Multiple

State	Inputs		Next state	Outputs												Comments
	Opcode	VCNZ		I	L	PS	DX	AX	BX	MB	FS	MD	RW	MM	M	
EX0	0010001	XXX	EX1	0	00	1000	0XXX	XXX	X	0000	1	1	X	0	LRI	R8 M[R[SA]], EX1
EX1	0010001	XXX	INF	0	01	0XXX	1000	XXX	X	0000	1	1	X	0	LRI	R[DR] M[R8], INF*
EX0	0001101	XXX0	EX1	0	00	1000	0XXX	XXX	X	0000	0	1	X	0	SRM	R8 R[SA], Z: EX1
EX0	0001101	XXX1	INF	0	01	1000	0XXX	XXX	X	0000	0	1	X	0	SRM	R8 R[SA], Z: INF*
EX1	0001101	XXX0	EX2	0	00	1001	XXXX	XXX	1	1100	0	1	X	0	SRM	R9 zf OP, Z: EX2
EX1	0001101	XXX1	INF	0	01	1001	XXXX	XXX	1	1100	0	1	X	0	SRM	R9 zf OP, Z: INF*
EX2	0001101	XXXX	EX3	0	00	1000	XXXX	1000	0	1101	0	1	X	0	SRM	R8 sr R8, EX3
EX3	0001101	XXX0	EX2	0	00	1001	1001	XXX	X	0110	0	1	X	0	SRM	R9 R9 1, Z: EX2
EX3	0001101	XXX1	EX4	0	00	1001	1001	XXX	X	0110	0	1	X	0	SRM	R9 R9 1, Z: EX4
EX4	0001101	XXXX	INF	0	01	0XXX	1000	XXX	X	0000	0	1	X	0	SRM	R[DR] R8, INF*
EX0	0001110	XXX0	EX1	0	00	1000	0XXX	XXX	X	0000	0	1	X	0	SLM	R8 R[SA], Z: EX1
EX0	0001110	XXX1	INF	0	01	1000	0XXX	XXX	X	0000	0	1	X	0	SLM	R8 R[SA], Z: INF*
EX1	0001110	XXX0	EX2	0	00	1001	XXXX	XXX	1	1100	0	1	X	0	SLM	R9 zf OP, Z: EX2
EX1	0001110	XXX1	INF	0	01	1001	XXXX	XXX	1	1100	0	1	X	0	SLM	R9 zf OP, Z: INF*
EX2	0001110	XXXX	EX3	0	00	1000	XXXX	1000	0	1110	0	1	X	0	SLM	R8 sl R8, EX3
EX3	0001110	XXX0	EX2	0	00	1001	1001	XXX	X	0110	0	1	X	0	SLM	R9 R9 1, Z: EX2
EX3	0001110	XXX1	EX4	0	00	1001	1001	XXX	X	0110	0	1	X	0	SLM	R9 R9 1, Z: EX4
EX4	0001110	XXXX	INF	0	01	0XXX	1000	XXX	X	0000	0	1	X	0	SLM	R[DR] R8, IF*

*For this state and input combination, PC ← PC + 1 also occurs.
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